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SLOPE GENERATOR WITH COMPENSATION OF TECHNOLOGY AND TEMPERATURE VARIATION FOR CURRENT LOOP INTERFACES

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Abstract
The objective of this paper is to present a new biasing circuit for current slope generation. The main advantage is obtaining stable transition duration of the slopes (TDS) independent of the technology process and temperature variations. The circuit can be used in different interface applications where a precise slope control is needed. The design is performed in 0.18um TSMC BCD technology using CAD system CADENCE.

Keywords – Current slope control, Output current generation, Current loop interfaces

1INTRODUCTION

The current loop interfaces are widely used for communications in automotive industry. One of the main challenges when such communication is used is the electromagnetic emissions occurring during the current slope. They are generated by the current slope distortions, proving that control of the current slope is required.

A schematic is shown for generating current slopes. A new way for compensation of technology and temperature variation is proposed in order to make the TDS accurate.

II. SLOPE GENERATION CIRCUIT

The block circuit that is used for controlling current TDS is illustrated in *Fig. 1.*

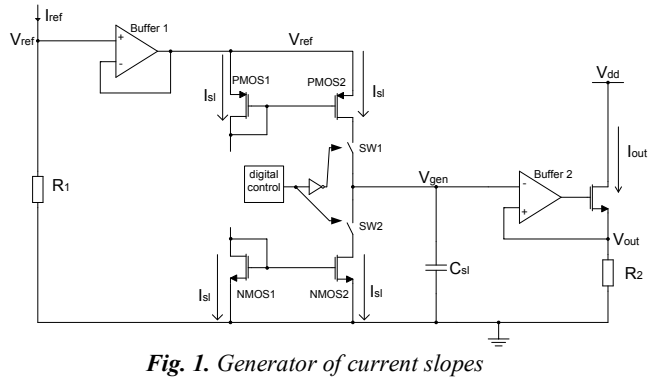

Fig. 1. *Generator of current slopes*

Current I_{ref} is injected in R_1 in order for V_{ref} to be formed. V_{ref} is buffered by Buffer1 and used for power supplying PMOS1 and PMOS2. A constant current I_{sl} is flowing through the PMOS and the NMOS current mirrors. The switch SW1 is used for charging capacitor C_{sl} with I_{sl} to the reference voltage V_{ref} and SW2 is used for discharging it to ground. The voltage over the capacitor is buffered by Buffer2 over R_2 in order for the output current to be generated. The steady state output current can be expressed by

$$I_{out} = \frac{R_1 I_{ref}}{R_2}, \qquad (1)$$

where R_1 is the same type poly resistor as R_2. It is clear that the temperature and the process dependences of the resistors value are neutralized and output current value is equal to scaled input reference current value. The equation for the TDS can be written as

$$t_{rise,fall} = \frac{C_{sl} V_{ref}}{I_{sl}} \qquad (2)$$

The voltage V_{out} is presented at *Fig. 2*.The voltage slope is generated when SW1 and SW2 toggle.

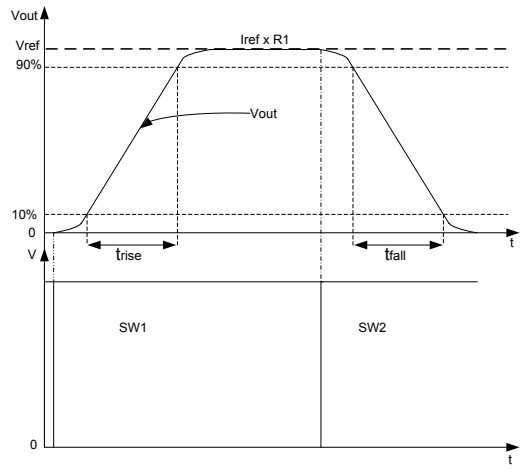

Fig. 2. *Generated voltage output pulse and digital control signals*

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III. COMPENSATION CIRCUIT

As can be seen in Eq.(2) the schematic does not solve the problem with the variation of V_{ref} and C_{sl} values. These values depend on process and temperature, which results in process and temperature instability for the current TDS.

One of the ways for compensating the variation, observed in Eq.(2) is making I_{sl} to depends on V_{ref} and C_{sl} values, the equation for I_{sl} should be

$$I_{sl} = k\, C_{sl} V_{ref} \qquad (3)$$

where k is a coefficient with dimension of $\frac{1}{time}$. To generate this dependent current, the circuit from *Fig. 3* is used.

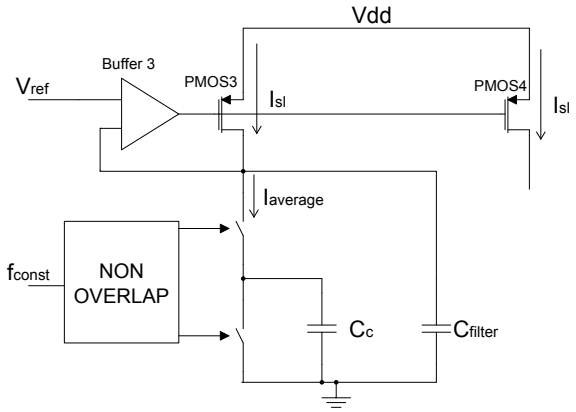

Fig. 3. *Circuit used for I_{sl} generation*

Resistor dependent voltage is applied by Buffer 3 over a capacitor, driven by a non-overlap circuit with frequency f_{const}. The voltage V_{ref} (*Fig.1*) could be used again, since it is resistor dependent voltage. The output current I_{sl} flows through the output PMOS3 transistor. The equation for I_{sl} is

$$I_{sl} = f_{const} C_c V_{ref} \qquad (4)$$

The slope transition equation can be written as

$$t_{rise,fall} = \frac{C_{sl} V_{ref}}{f_{sconst} V_{ref} C_c} \qquad (5)$$

When $C_c = C_{sl}$, Eq.(5) simplifies to Eq.(6):

$$t_{rise,fall} = \frac{1}{f_{const}} \qquad (6)$$

It is clear that the accuracy of the slopes $t_{rise,fall}$ strongly depends on the accuracy of applied frequency $f_{const.}$

IV. CIRCUIT IMPLEMENTATION

The gain-bandwidth (GBW) of Buffer1 in *Fig.1* is 50MHz which helps transistor PMOS2 not to be in saturation by the voltage fall when the raising slope occurs. That will result in distorted slopes. The voltage drain-source V_{DS} of transistor PMOS2 is illustrated at *Fig.4*.

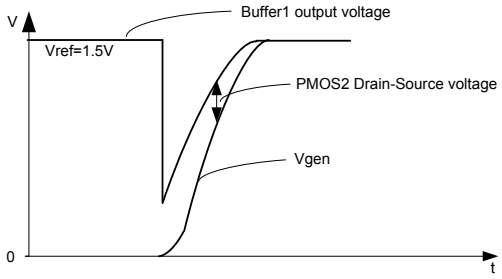

Fig. 4. *V_{gen} transition when rising slope occurs*

In the circuit SW1 and SW2 are CMOS switches designed in a way to minimize their capacitance C_{GS}, thus reduce parasitic peaks in the voltage over the capacitor C_{sl}. Its value has to be bigger than 3pF in order to eliminate the high order effects over slope distortion.

Some requirements related the buffers in the schematic are presented below. The Buffer2 in *Fig.1* should be made with wider gain-bandwidth in order to repeat the V_{gen} accurately. The operational amplifier used for this buffer has GBW of 10MHz. This amplifier repeats the slopes asymmetrically with a delay for the rising and falling slope. This delay gives spope variation of about 15%, compared to the slopes of V_{gen}. A faster operational amplifier is required in order to keep this error low. The operational amplifier that is used for Buffer3 has GBW=10kHz, since its GBW should be at least 100 times lower than f_{const} otherwise there will be stability issues. The value of C_{filter} should be bigger than value of C_c no more than ten times. This is necessary to ensure good filtering of the voltage over C_c and needed AC stability of the Buffer3.

V. SIMULATION RESULTS

The circuit is designed on 0.18μm TSMC technology and simulated using Spectre simulator for typical (tt) and worst case slow and fast models (ss, sf, fs, ff).

The power supply Vdd is 4V and the reference current I_{ref} is10μA. To achieve target value for $t_{rise,fall}$ of *500ns*, the following values of devices in *Fig.1 and Fig.3* are used: C_{sl}=*2.8pF*, R_1=*150kΩ*, I_{ref}=*10μA*, $\frac{R_1}{R_2} = 1500$, in *Fig.3*: C_c=*0.7pF* C_{filter}=*3.5pF*. The frequency of the non-overlapping circuit is 8MHz.

The ratio between PMOS1 and PMOS2 in *Fig.1* and between PMOS3 and PMOS4 in *Fig. 3*, ensures different TDS. For the presented simulation this ratio is one.

As results for the output current TDS depends very much on Buffer2 GBW value, only results for the rising voltage slope over C_{sl} would be presented. The results for the falling slope are symmetrical.

The simulation results for steady state current *Iout* and rising slope *trise* are summarized in Table.2. The typical values of the parameters are obtained at typical process and temperature of 27ºC.

TABLE 2.SIMULATION RESULTS

Simulation type	t_{rise} *typ [ns]*	t_{rise} *max [ns]*	t_{rise} *min [ns]*	I_{out} *typ [mA]*	I_{out} *max [mA]*	I_{out} *min [mA]*
Process and temperature	491	502	476	15	15.41	14.55
Monte Carlo, process and temperature	491	σ =8.5	σ =-9	15	σ =0.2	σ =-0.2

The variation of t_{rise} is graphically presented in *Fig. 5*. The temperature varies from -50ºC and 160ºC.

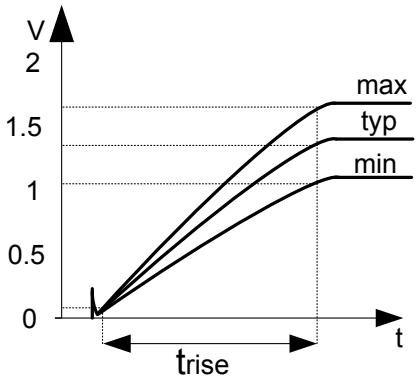

Fig. 5. *V_{gen} transition when rising slope occurs*

Due to significant variation of V_{ref} the steady state voltage over C_{sl} varies ±60%. The maximum and minimum values are achieved at low temperature and slow process model, and respectively at high temperature and fast process model. When the slope starts to rise it is distorted by SW1's C_{GS} parasitic capacitance.

Monte Carlo simulation is also performed using models for Gaussian mismatch for all devices and Gaussian process distribution. The results are defined by $\frac{C_{sl}}{C_c}$ mismatch ratio and the mismatch ratios of all current mirrors through which I_{sl} flows. If different value of resistor is used for V_{ref} generation in the schematic in *Fig.3* other than R_1, the mismatch between this resistor and R_1 will also result in a high $t_{rise,fall}\sigma$.

The results for the current I_{out} through R_2 are defined by the ratio $\frac{R_1}{R_2}$ and the value of the I_{ref} current.

V. CONCLUSION

In this paper, a circuit for current slope generation was proposed. The design was simulated in 0.18µm TSMC technology. The parameters and characteristics of the schematic depend mainly on matching between devices. Problems with TDS variation in the generator of the current slopes are analyzed and a solution is presented.

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